FIG. 1

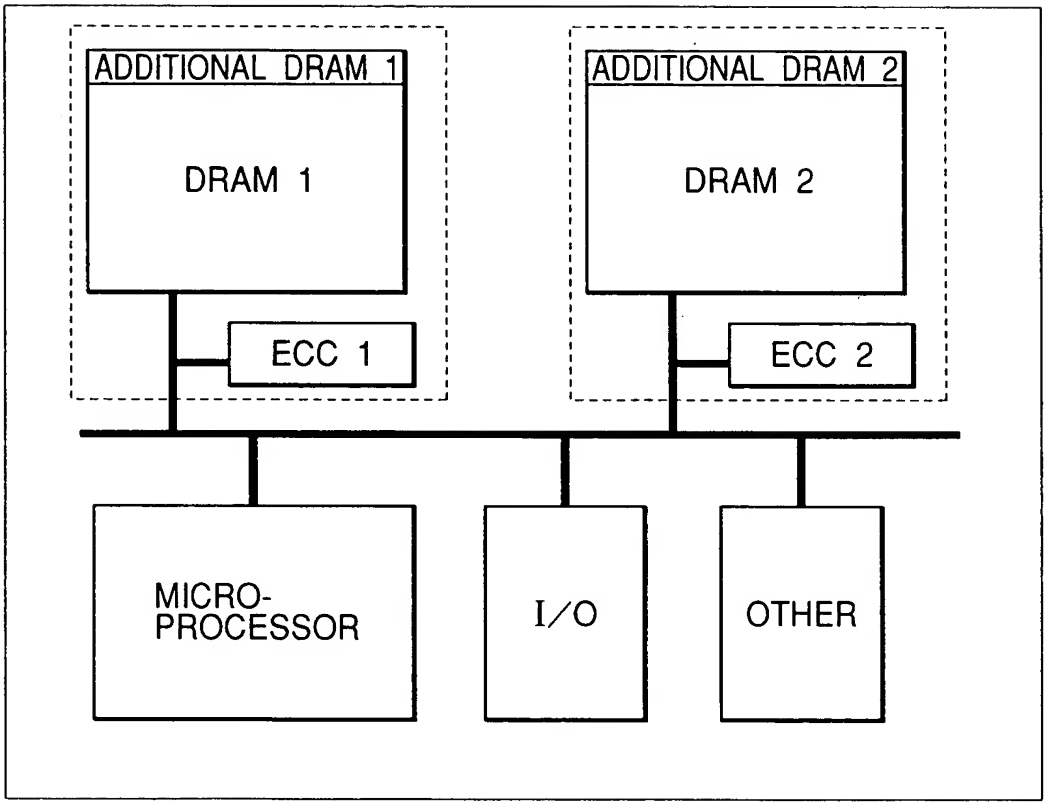

ADDITIONAL DRAM 1
DRAM 1
ECC 1
ADDITIONAL DRAM 2
DRAM 2
ECC 2
MICRO-
PROCESSOR
I/O
OTHER

FIG. 2

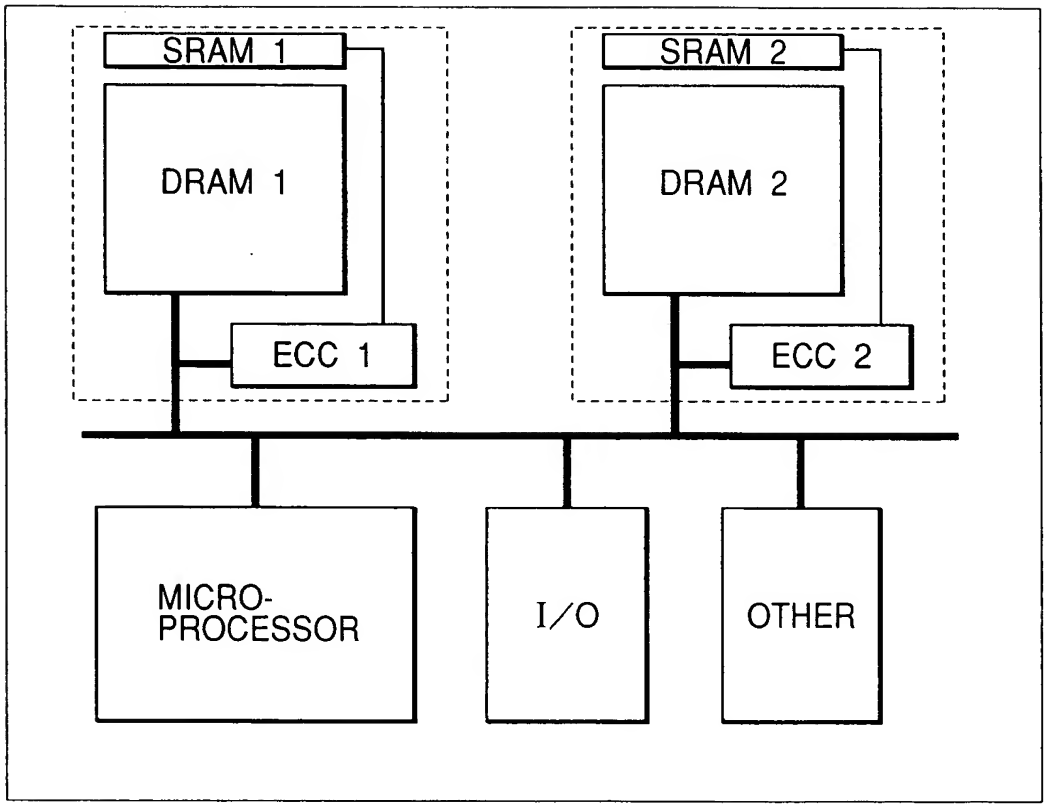


FIG. 3

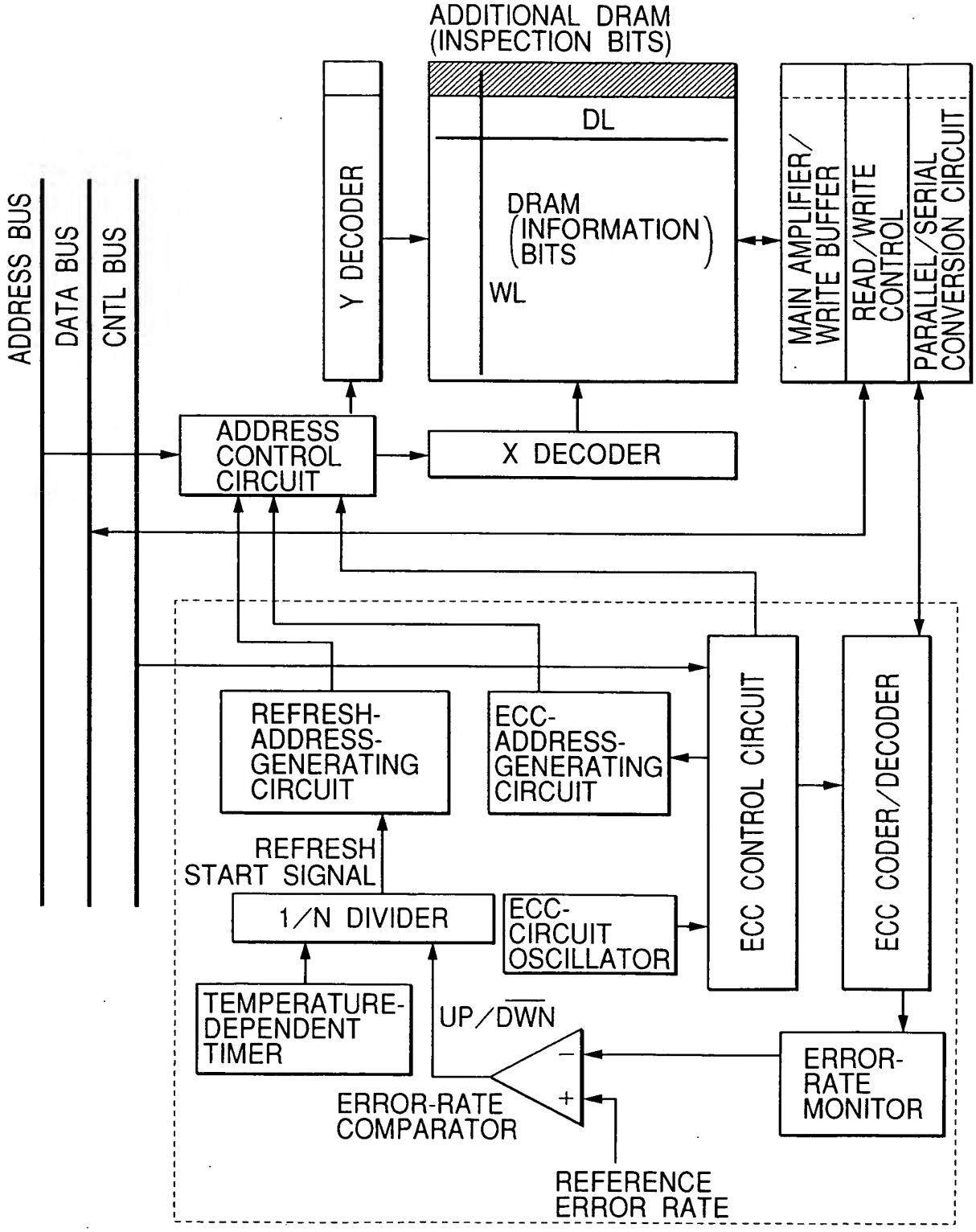

ADDITIONAL DRAM
(INSPECTION BITS)
DL
DRAM
(INFORMATION
BITS)
WL
Y DECODER
X DECODER
ADDRESS BUS
DATA BUS
CNTL BUS
ADDRESS
CONTROL
CIRCUIT
MAIN AMPLIFIER/
WRITE BUFFER
READ/WRITE
CONTROL
PARALLEL/SERIAL
CONVERSION CIRCUIT
REFRESH-
ADDRESS-
GENERATING
CIRCUIT
ECC-
ADDRESS-
GENERATING
CIRCUIT
ECC CONTROL CIRCUIT
ECC CODER/DECODER
REFRESH
START SIGNAL
1/N DIVIDER
ECC-
CIRCUIT
OSCILLATOR
TEMPERATURE-
DEPENDENT
TIMER
UP/DWN
ERROR-
RATE
MONITOR
ERROR-RATE
COMPARATOR
REFERENCE
ERROR RATE

FIG. 4

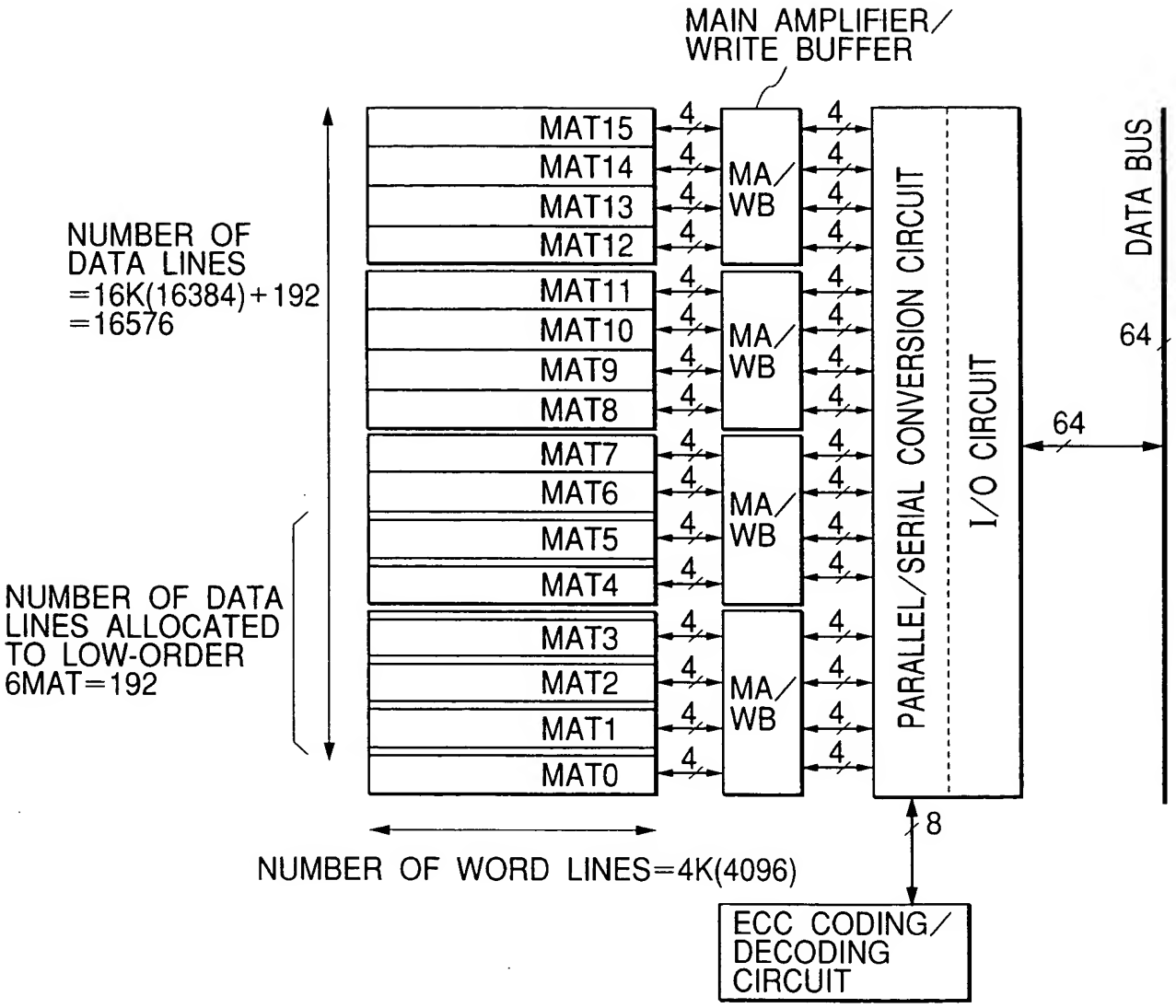

MAIN AMPLIFIER/
WRITE BUFFER
NUMBER OF
DATA LINES
=16K(16384)+192
=16576
NUMBER OF DATA
LINES ALLOCATED
TO LOW-ORDER
6MAT=192
MAT15
MAT14
MAT13
MAT12
MAT11
MAT10
MAT9
MAT8
MAT7
MAT6
MAT5
MAT4
MAT3
MAT2
MAT1
MAT0
MA/
WB
MA/
WB
MA/
WB
MA/
WB
4
PARALLEL/SERIAL CONVERSION CIRCUIT
I/O CIRCUIT
64
DATA BUS
64
8
NUMBER OF WORD LINES=4K(4096)
ECC CODING/
DECODING
CIRCUIT

FIG. 5

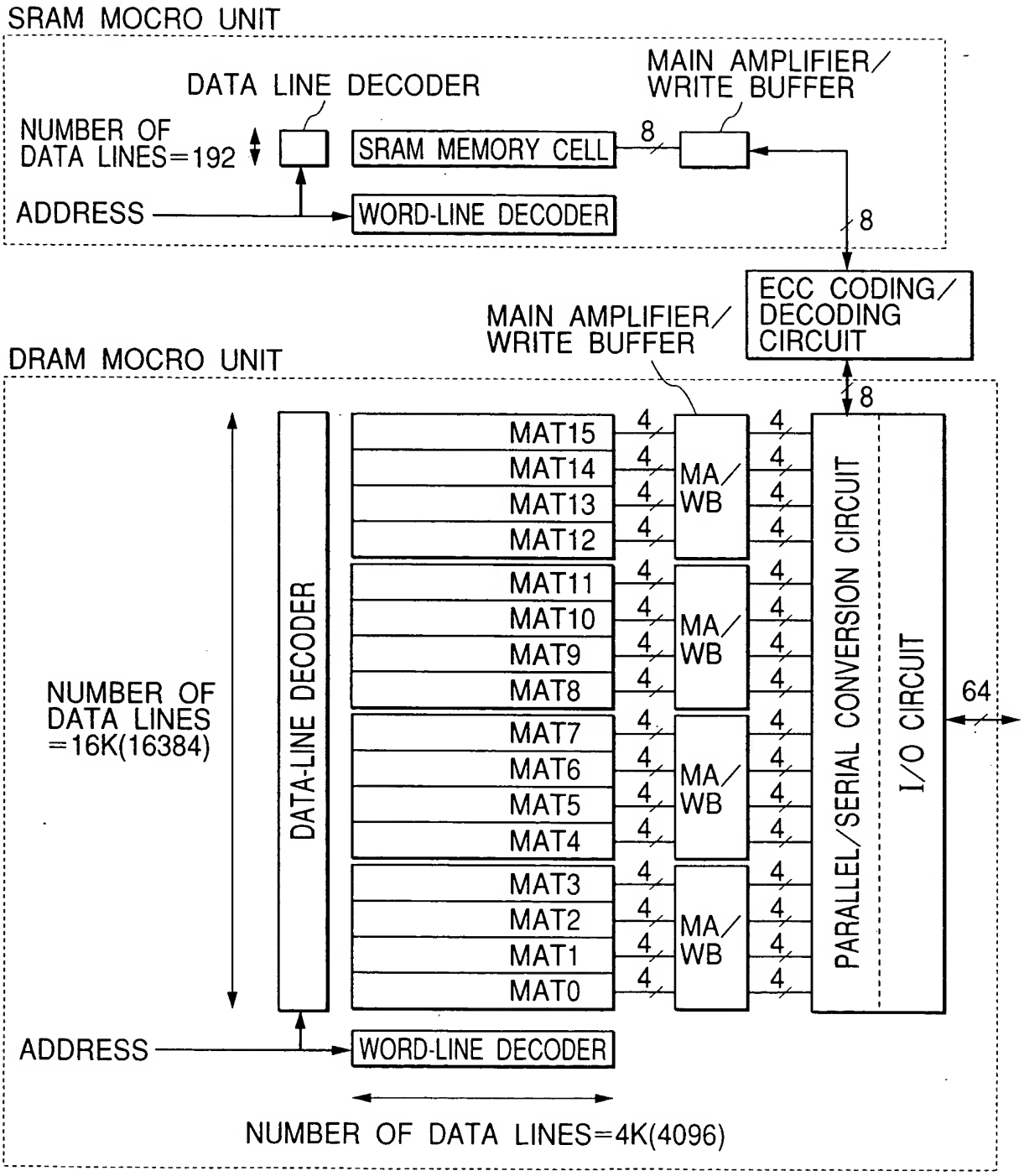

SRAM MOCRO UNIT
DATA LINE DECODER
MAIN AMPLIFIER/
WRITE BUFFER
NUMBER OF
DATA LINES=192
SRAM MEMORY CELL
8
ADDRESS
WORD-LINE DECODER
8
ECC CODING/
DECODING
CIRCUIT
MAIN AMPLIFIER/
WRITE BUFFER
DRAM MOCRO UNIT
8
MAT15
MAT14
MAT13
MAT12
MAT11
MAT10
MAT9
MAT8
MAT7
MAT6
MAT5
MAT4
MAT3
MAT2
MAT1
MAT0
4
MA/
WB
PARALLEL/SERIAL CONVERSION CIRCUIT
I/O CIRCUIT
64
NUMBER OF
DATA LINES
=16K(16384)
DATA-LINE DECODER
ADDRESS
WORD-LINE DECODER
NUMBER OF DATA LINES=4K(4096)

FIG. 6

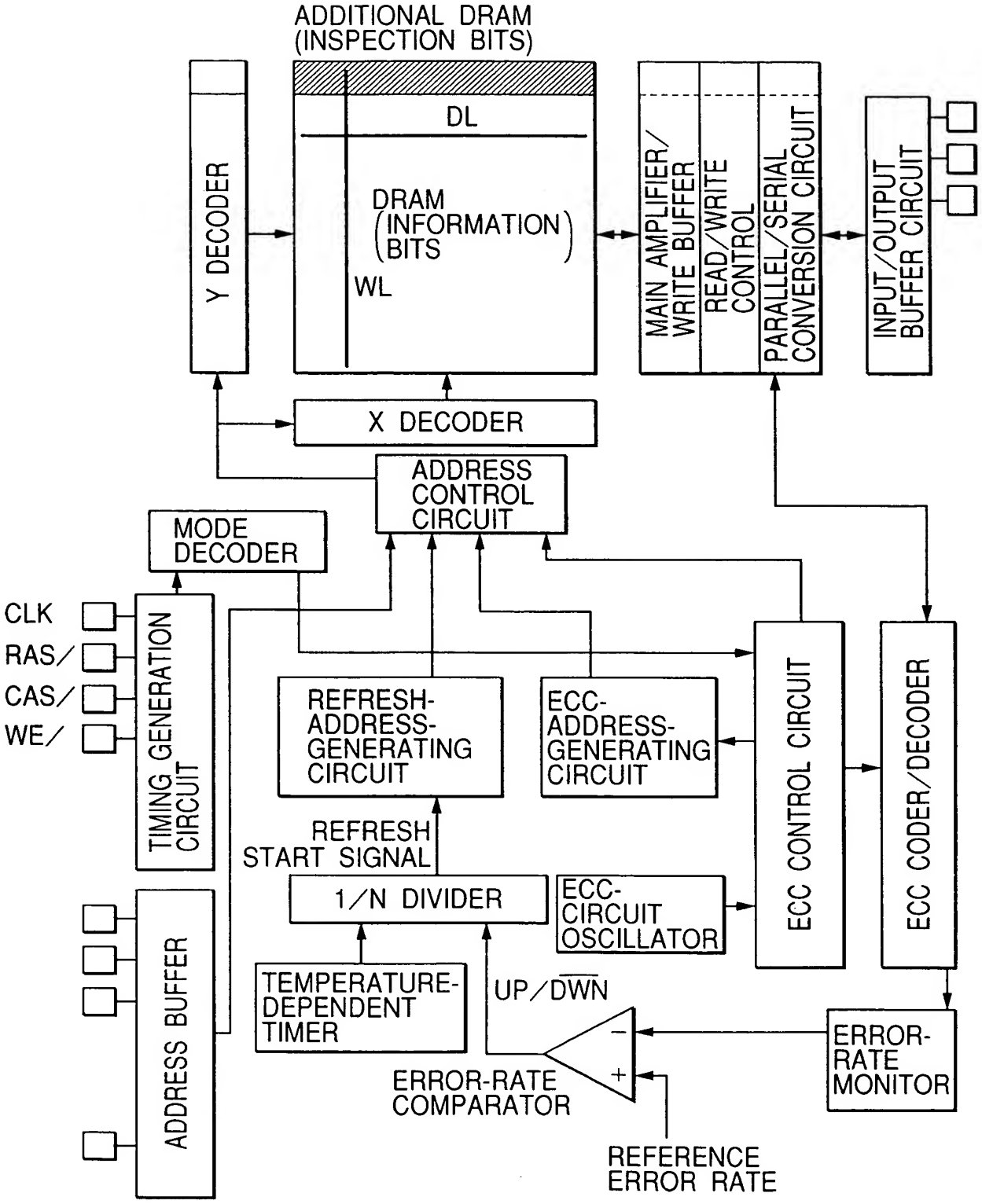

ADDITIONAL DRAM
(INSPECTION BITS)
DL
DRAM
(INFORMATION
BITS)
WL
Y DECODER
MAIN AMPLIFIER/
WRITE BUFFER
READ/WRITE
CONTROL
PARALLEL/SERIAL
CONVERSION CIRCUIT
INPUT/OUTPUT
BUFFER CIRCUIT
X DECODER
ADDRESS
CONTROL
CIRCUIT
MODE
DECODER
CLK
RAS/
CAS/
WE/
TIMING GENERATION
CIRCUIT
REFRESH-
ADDRESS-
GENERATING
CIRCUIT
ECC-
ADDRESS-
GENERATING
CIRCUIT
ECC CONTROL CIRCUIT
ECC CODER/DECODER
REFRESH
START SIGNAL
1/N DIVIDER
ECC-
CIRCUIT
OSCILLATOR
ADDRESS BUFFER
TEMPERATURE-
DEPENDENT
TIMER
UP/DWN
ERROR-
RATE
MONITOR
ERROR-RATE
COMPARATOR
REFERENCE
ERROR RATE

FIG. 7

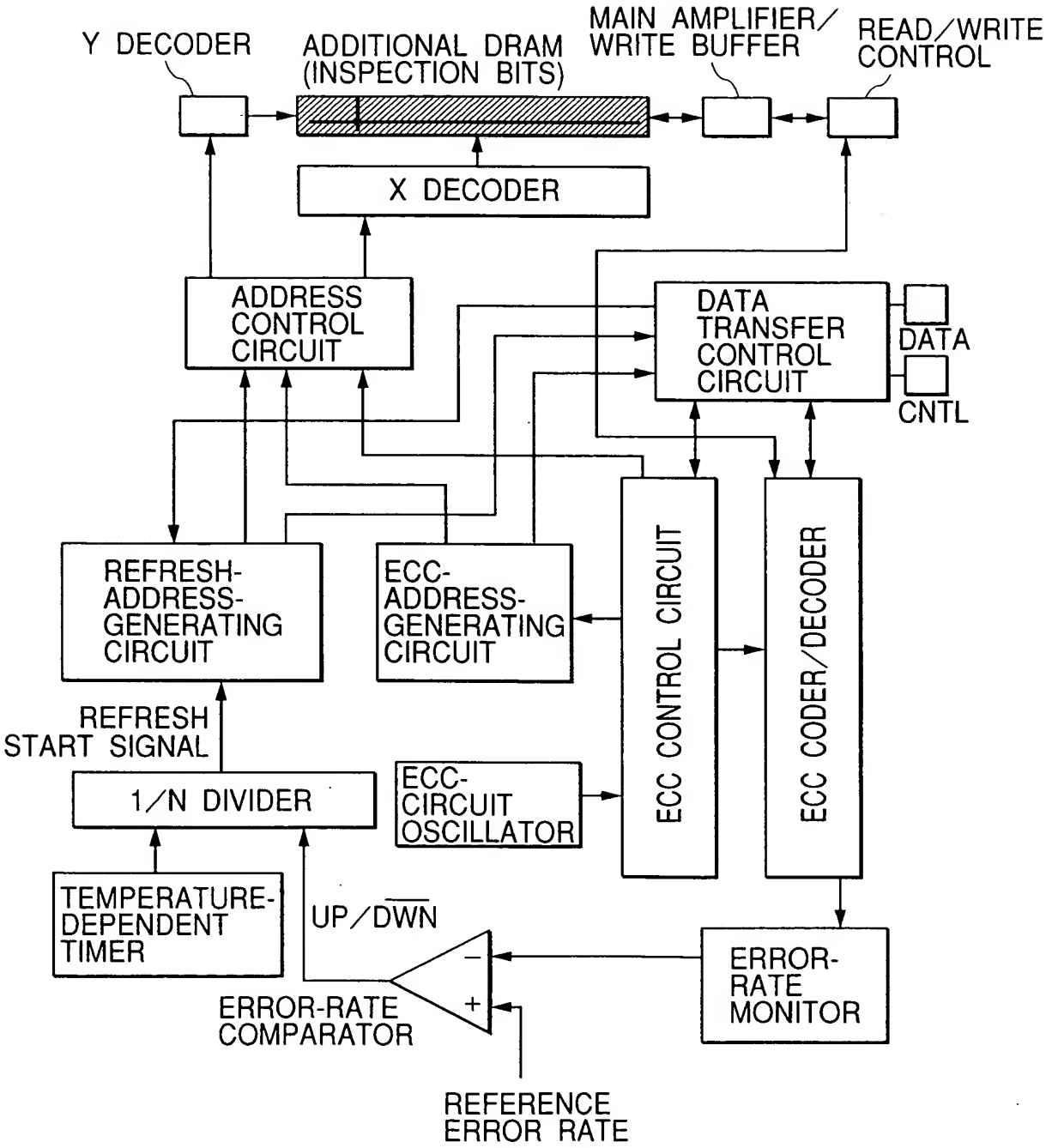

Y DECODER
ADDITIONAL DRAM (INSPECTION BITS)
MAIN AMPLIFIER/ WRITE BUFFER
READ/WRITE CONTROL
X DECODER
ADDRESS CONTROL CIRCUIT
DATA TRANSFER CONTROL CIRCUIT
DATA
CNTL
REFRESH-ADDRESS-GENERATING CIRCUIT
ECC-ADDRESS-GENERATING CIRCUIT
ECC CONTROL CIRCUIT
ECC CODER/DECODER
REFRESH START SIGNAL
1/N DIVIDER
ECC-CIRCUIT OSCILLATOR
TEMPERATURE-DEPENDENT TIMER
UP/DWN
ERROR-RATE MONITOR
ERROR-RATE COMPARATOR
REFERENCE ERROR RATE

FIG. 8

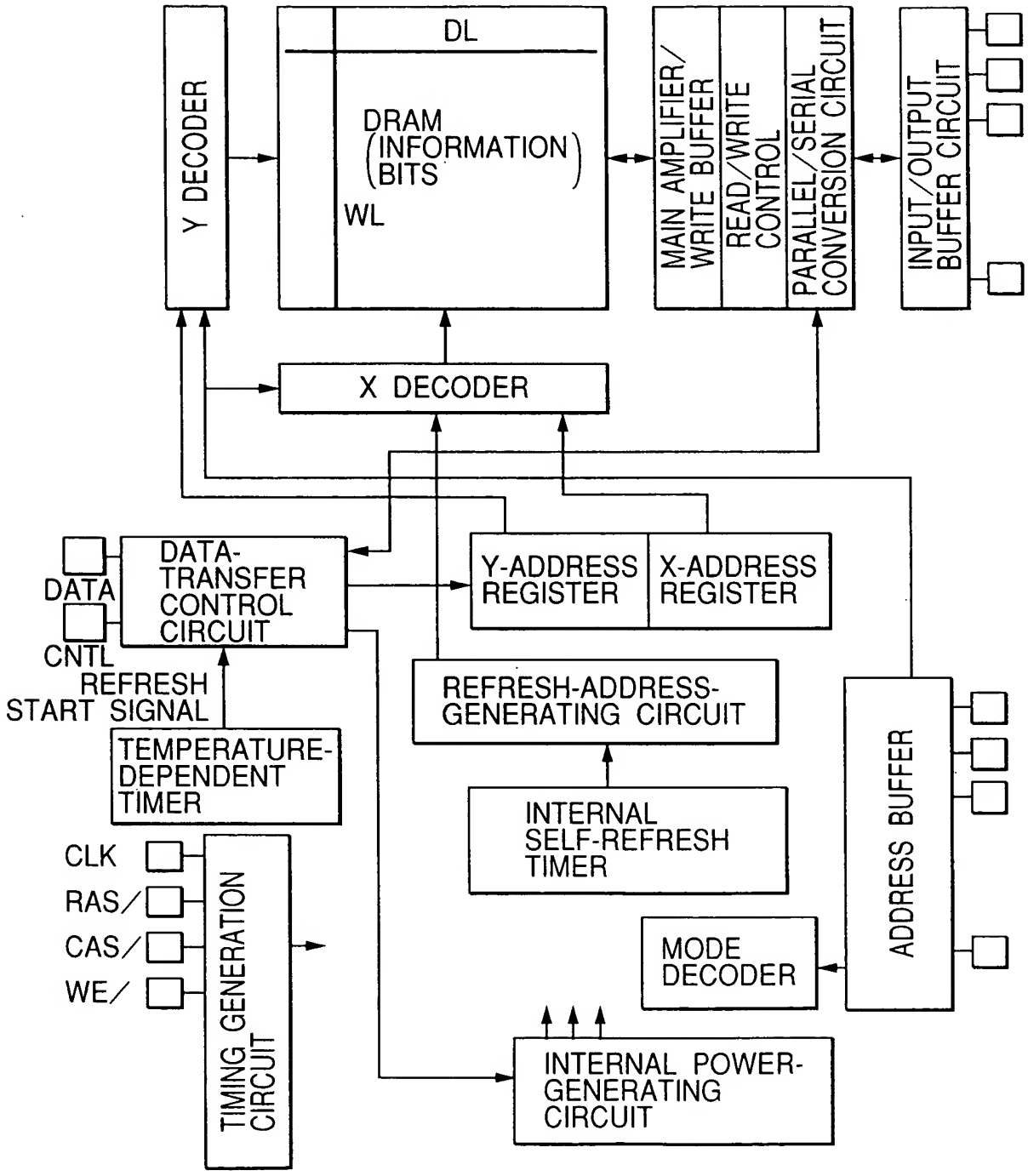

Y DECODER
DL
DRAM
(INFORMATION
BITS)
WL
MAIN AMPLIFIER/
WRITE BUFFER
READ/WRITE
CONTROL
PARALLEL/SERIAL
CONVERSION CIRCUIT
INPUT/OUTPUT
BUFFER CIRCUIT
X DECODER
DATA
CNTL
DATA-
TRANSFER
CONTROL
CIRCUIT
Y-ADDRESS
REGISTER
X-ADDRESS
REGISTER
REFRESH
START SIGNAL
TEMPERATURE-
DEPENDENT
TIMER
REFRESH-ADDRESS-
GENERATING CIRCUIT
INTERNAL
SELF-REFRESH
TIMER
ADDRESS BUFFER
CLK
RAS/
CAS/
WE/
TIMING GENERATION
CIRCUIT
MODE
DECODER
INTERNAL POWER-
GENERATING
CIRCUIT

FIG. 9

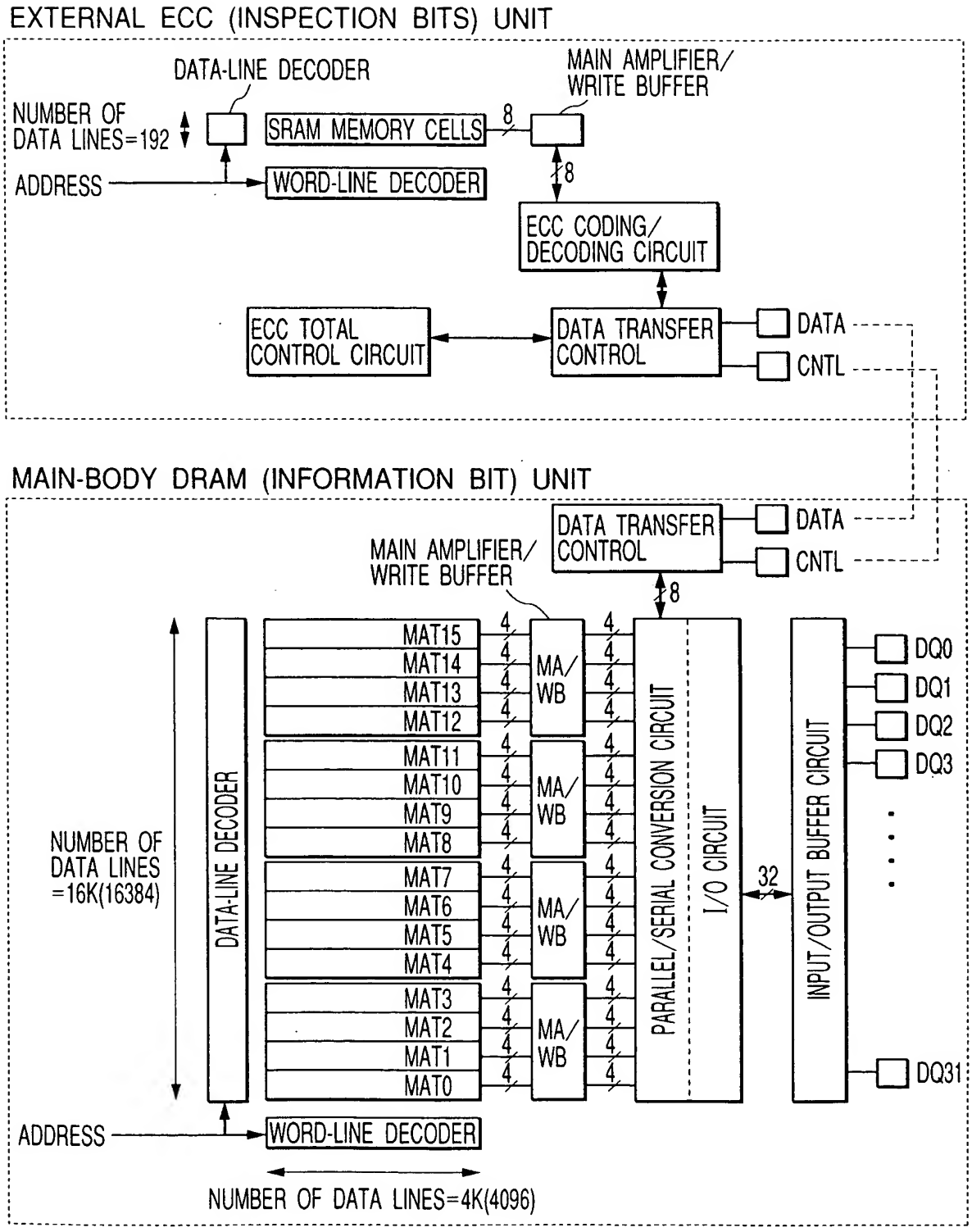

EXTERNAL ECC (INSPECTION BITS) UNIT
DATA-LINE DECODER
MAIN AMPLIFIER/
WRITE BUFFER
NUMBER OF
DATA LINES=192
SRAM MEMORY CELLS
8
ADDRESS
WORD-LINE DECODER
8
ECC CODING/
DECODING CIRCUIT
ECC TOTAL
CONTROL CIRCUIT
DATA TRANSFER
CONTROL
DATA
CNTL
MAIN-BODY DRAM (INFORMATION BIT) UNIT
DATA TRANSFER
CONTROL
DATA
CNTL
MAIN AMPLIFIER/
WRITE BUFFER
8
MAT15
MAT14
MAT13
MAT12
MAT11
MAT10
MAT9
MAT8
MAT7
MAT6
MAT5
MAT4
MAT3
MAT2
MAT1
MAT0
4
MA/
WB
PARALLEL/SERIAL CONVERSION CIRCUIT
I/O CIRCUIT
32
INPUT/OUTPUT BUFFER CIRCUIT
DQ0
DQ1
DQ2
DQ3
DQ31
NUMBER OF
DATA LINES
=16K(16384)
DATA-LINE DECODER
ADDRESS
WORD-LINE DECODER
NUMBER OF DATA LINES=4K(4096)

FIG. 10

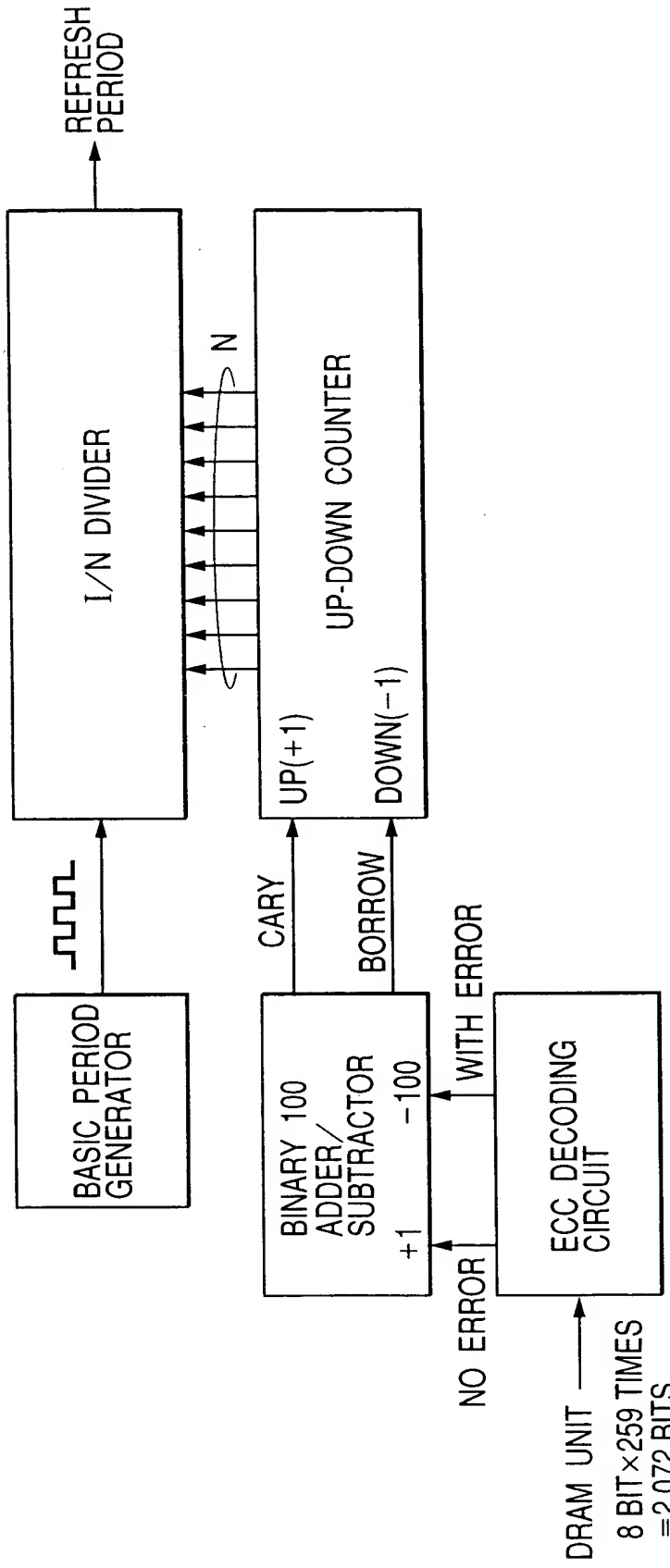

REFRESH PERIOD
I/N DIVIDER
N
UP-DOWN COUNTER
UP(+1)
DOWN(−1)
BASIC PERIOD GENERATOR
CARY
BORROW
BINARY 100 ADDER/ SUBTRACTOR
−100
+1
WITH ERROR
NO ERROR
ECC DECODING CIRCUIT
DRAM UNIT
8 BIT×259 TIMES =2,072 BITS

FIG. 11

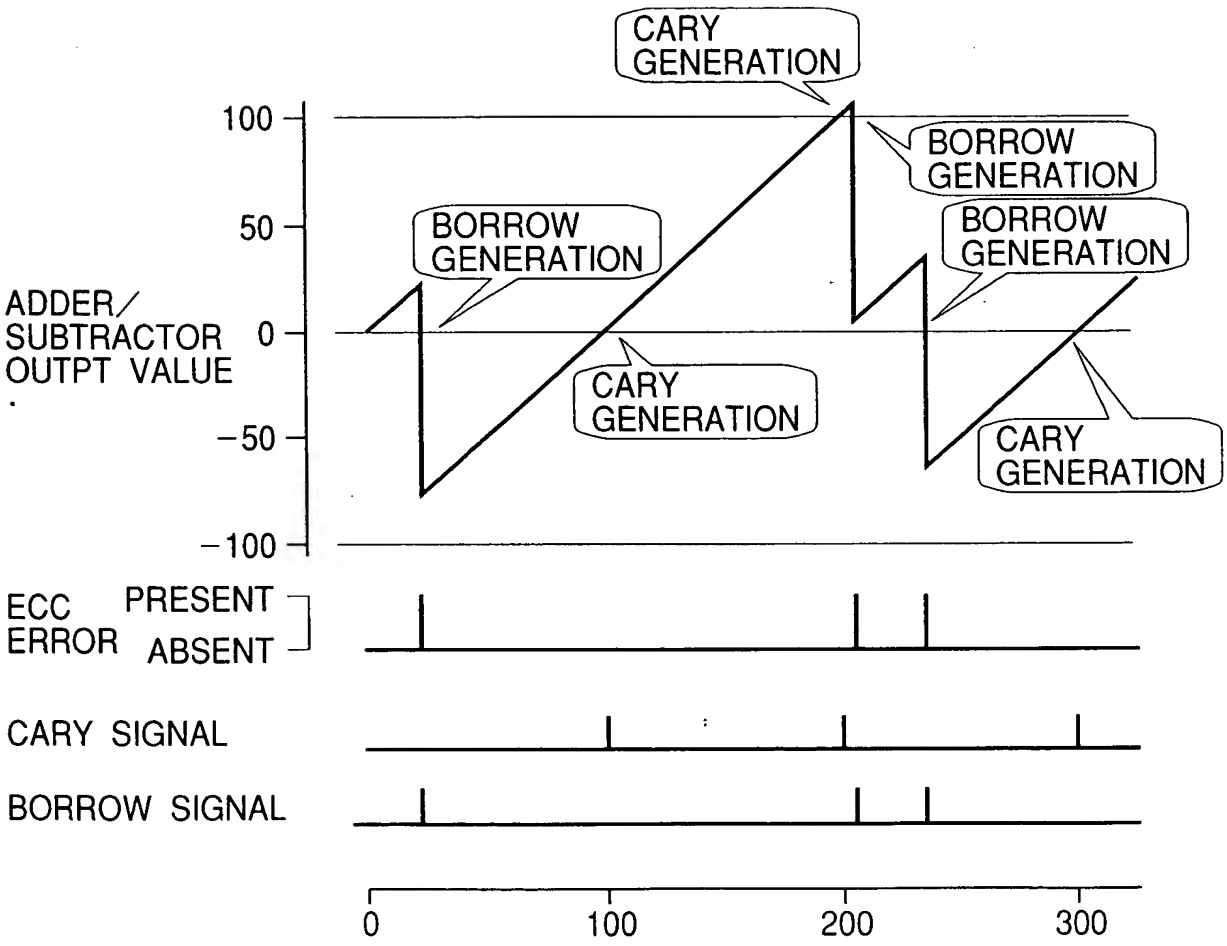

CARY GENERATION
BORROW GENERATION
BORROW GENERATION
BORROW GENERATION
CARY GENERATION
CARY GENERATION
100
50
0
−50
−100
ADDER/ SUBTRACTOR OUTPT VALUE
ECC ERROR
PRESENT
ABSENT
CARY SIGNAL
BORROW SIGNAL
0
100
200
300

FIG. 12

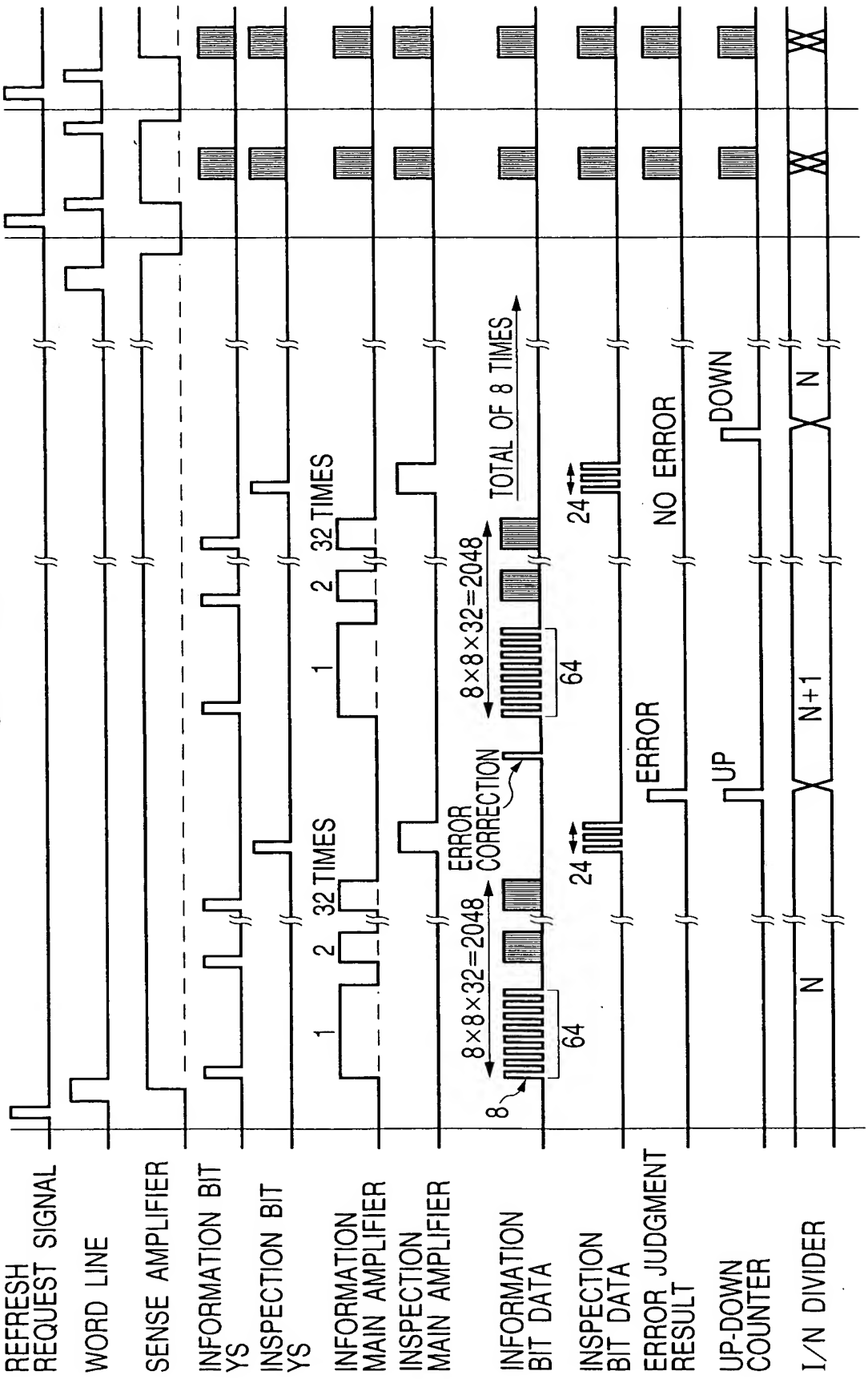

REFRESH REQUEST SIGNAL
WORD LINE
SENSE AMPLIFIER
INFORMATION BIT YS
INSPECTION BIT YS
INFORMATION MAIN AMPLIFIER
INSPECTION MAIN AMPLIFIER
INFORMATION BIT DATA
INSPECTION BIT DATA
ERROR JUDGMENT RESULT
UP-DOWN COUNTER
I/N DIVIDER
1
2
32 TIMES
8×8×32=2048
64
8
ERROR CORRECTION
TOTAL OF 8 TIMES
24
ERROR
NO ERROR
UP
DOWN
N
N+1

FIG. 13

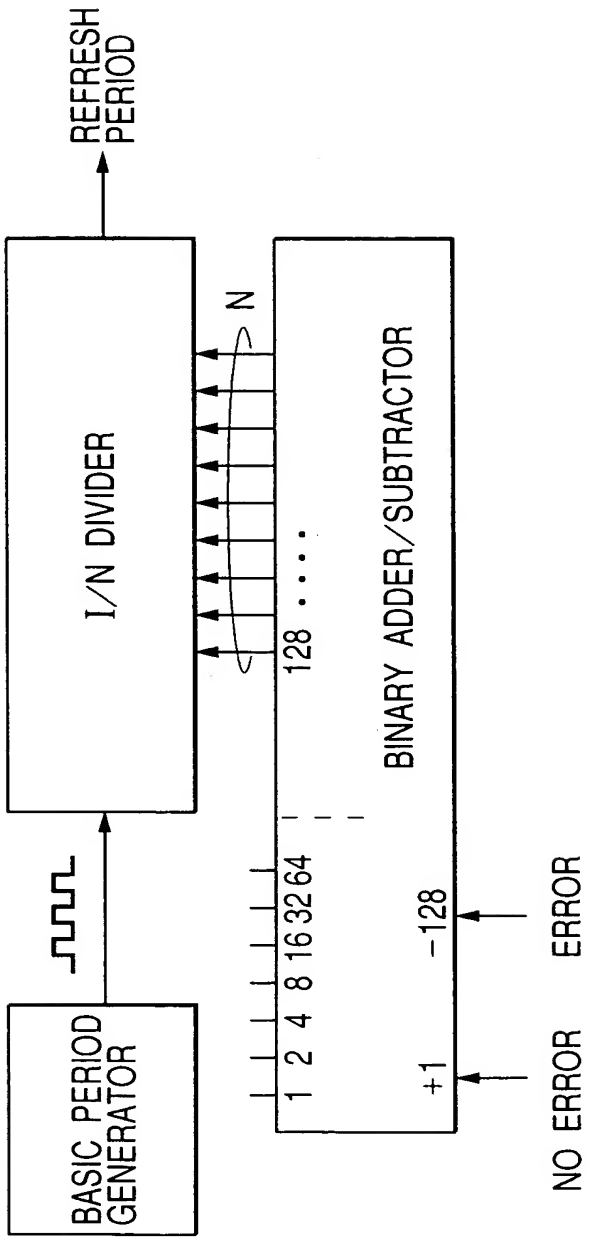

REFRESH PERIOD
I/N DIVIDER
N
128 ....
BINARY ADDER/SUBTRACTOR
1 2 4 8 16 32 64
-128
+1
BASIC PERIOD GENERATOR
NO ERROR
ERROR

FIG. 14

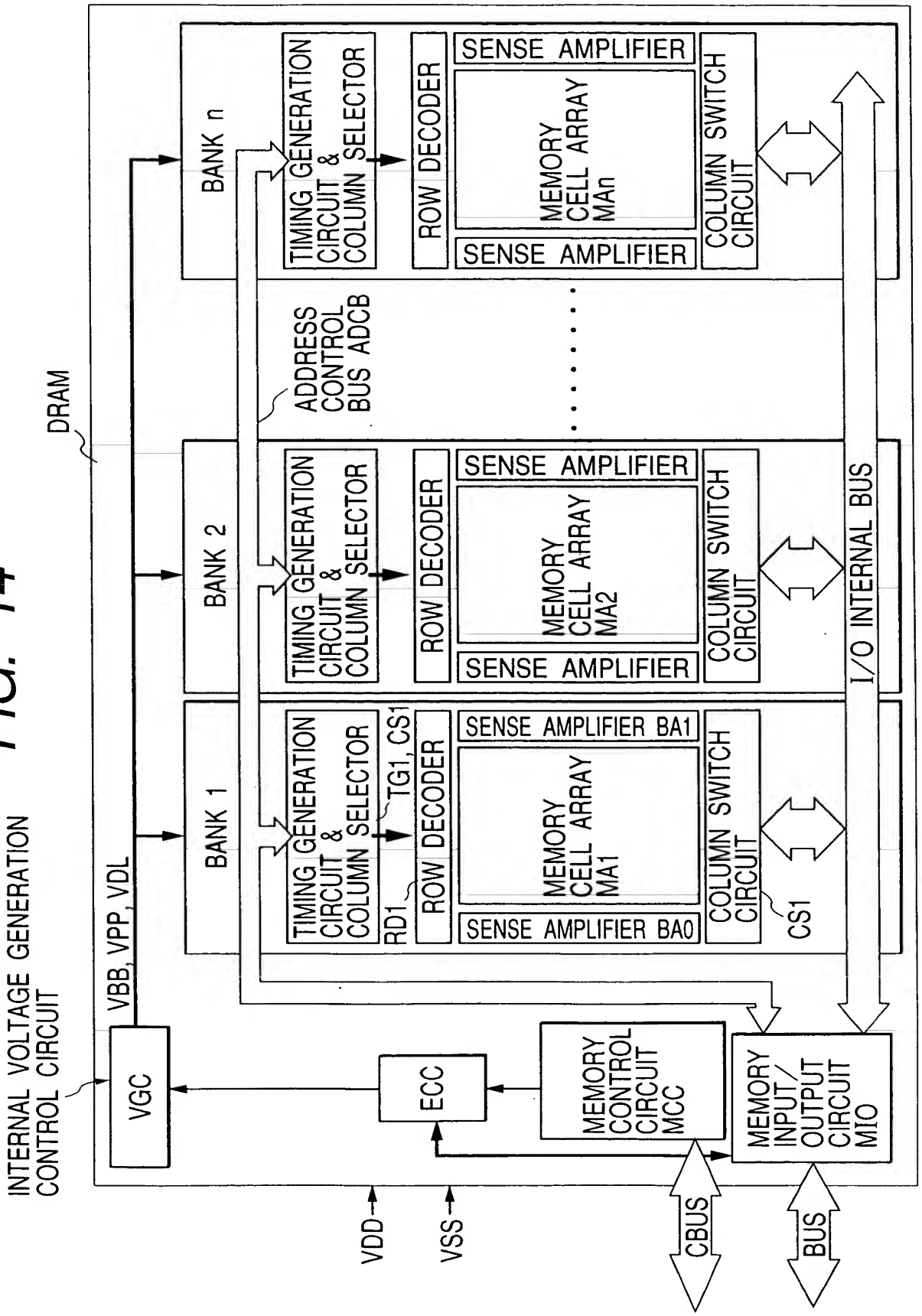

DRAM
INTERNAL VOLTAGE GENERATION CONTROL CIRCUIT
VGC
VBB, VPP, VDL
BANK 1
BANK 2
BANK n
TIMING GENERATION CIRCUIT & COLUMN SELECTOR
TG1, CS1
RD1
ROW DECODER
SENSE AMPLIFIER BA1
SENSE AMPLIFIER BA0
SENSE AMPLIFIER
MEMORY CELL ARRAY MA1
MEMORY CELL ARRAY MA2
MEMORY CELL ARRAY MAn
COLUMN SWITCH CIRCUIT
CS1
ADDRESS CONTROL BUS ADCB
I/O INTERNAL BUS
ECC
MEMORY CONTROL CIRCUIT MCC
MEMORY INPUT/OUTPUT CIRCUIT MIO
VDD
VSS
CBUS
BUS

FIG. 15

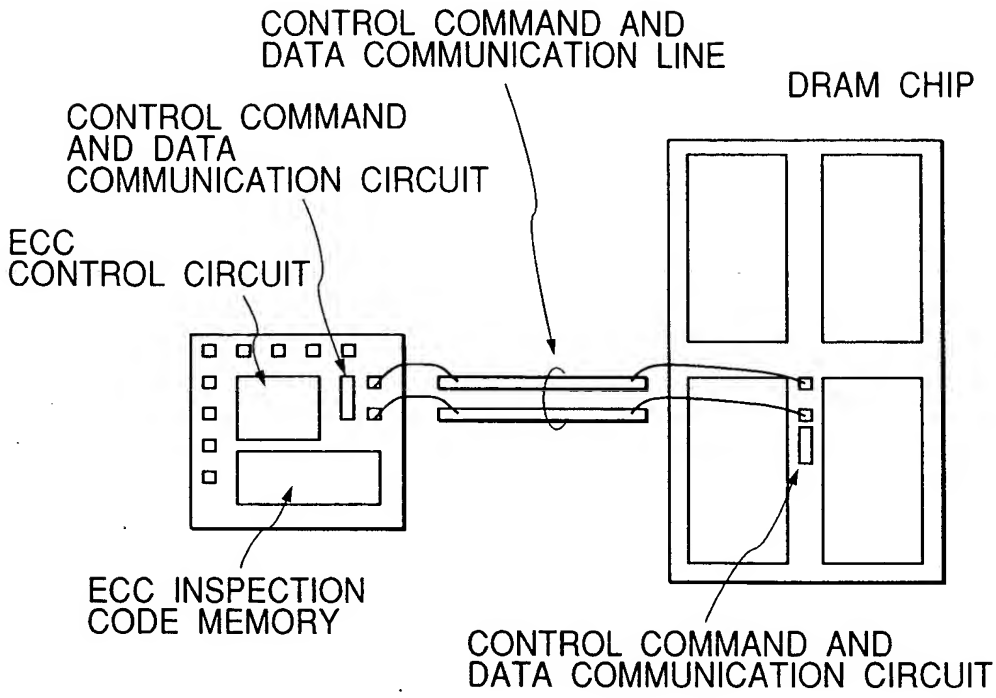


FIG. 16(A)

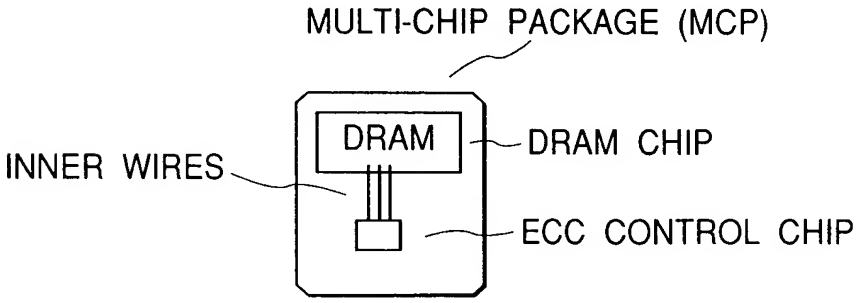


FIG. 16(B)

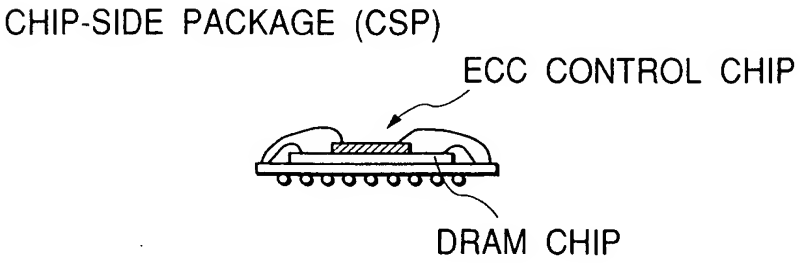


FIG. 17

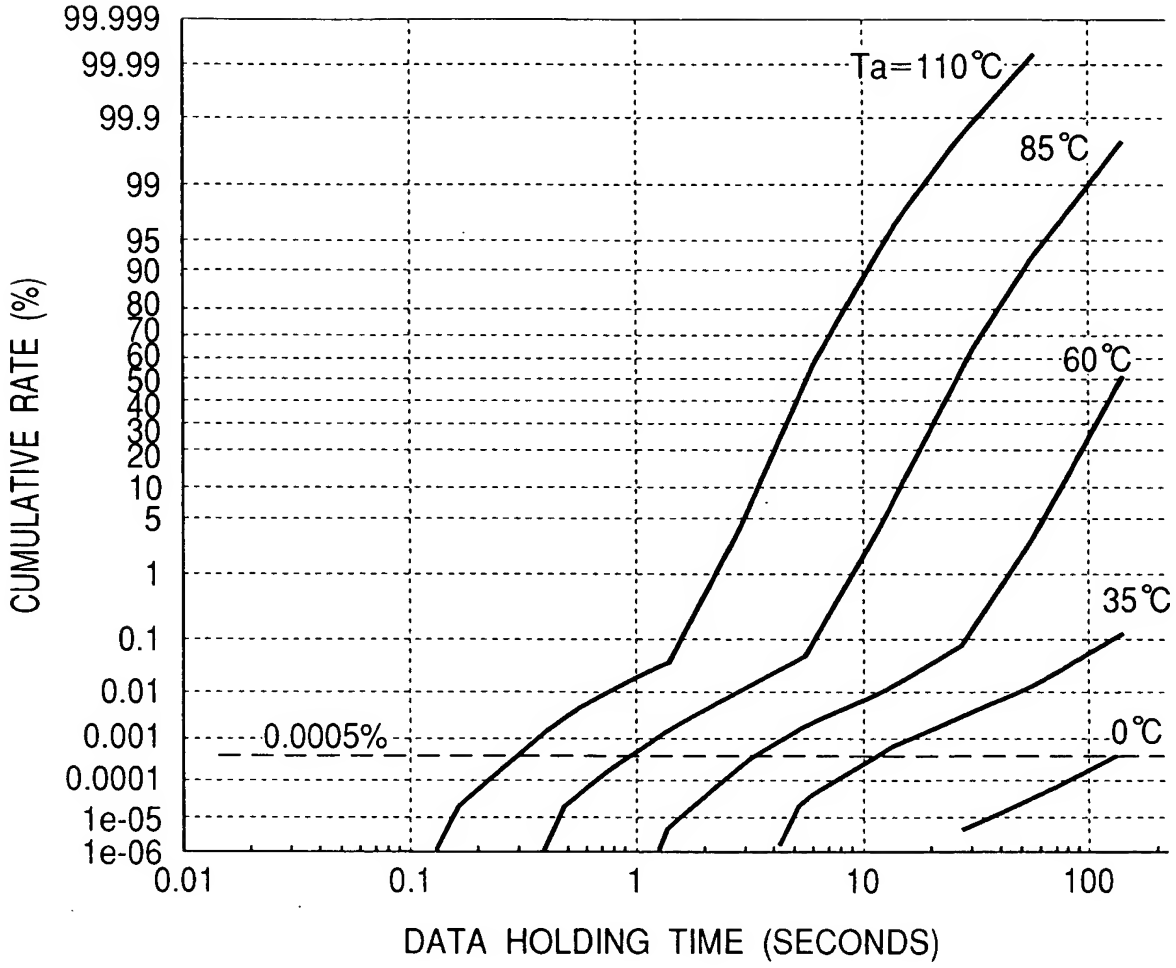
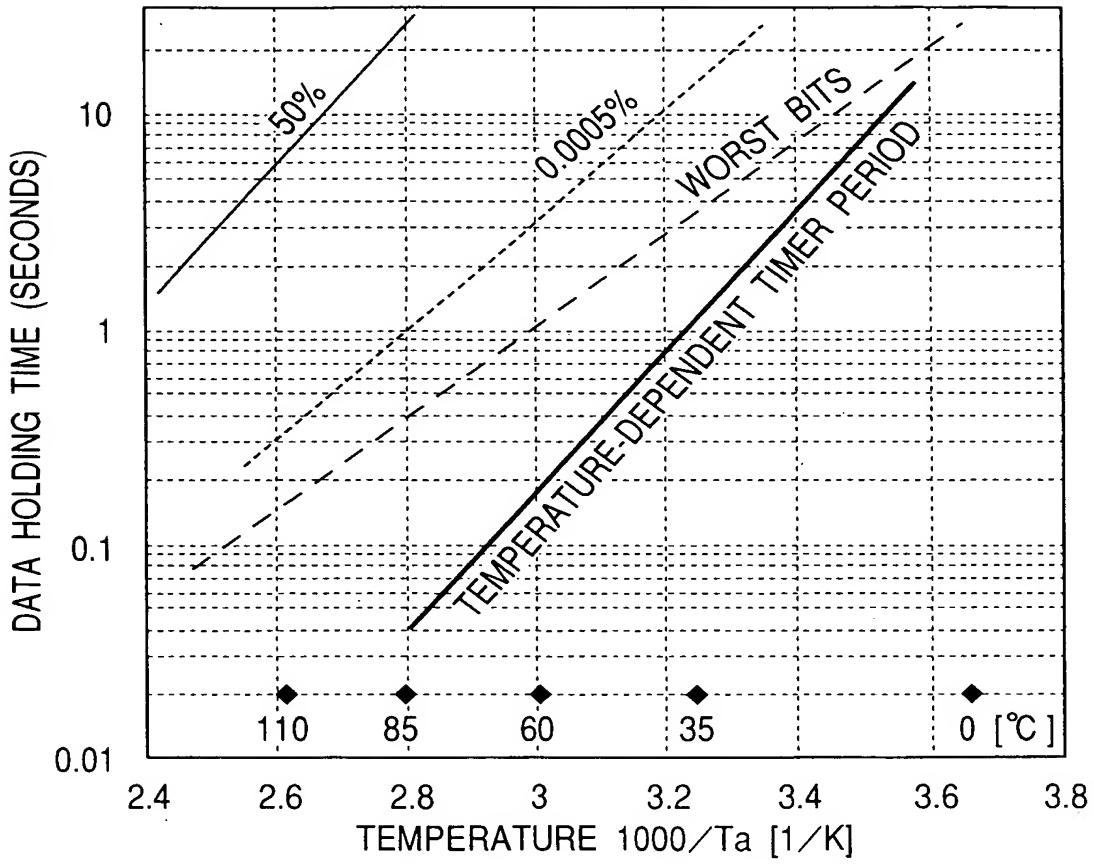

99.999
99.99
99.9
99
95
90
80
70
60
50
40
30
20
10
5
1
0.1
0.01
0.001
0.0001
1e-05
1e-06
CUMULATIVE RATE (%)
0.01
0.1
1
10
100
DATA HOLDING TIME (SECONDS)
Ta=110℃
85℃
60℃
35℃
0℃
0.0005%

FIG. 18


DATA HOLDING TIME (SECONDS)
10
1
0.1
0.01
50%
0.0005%
WORST BITS
TEMPERATURE-DEPENDENT TIMER PERIOD
110
85
60
35
0 [℃]
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
TEMPERATURE 1000/Ta [1/K]